Semiconductor
March 1997

82C82
CMOS Octal Latching Bus Driver

Features
- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8282 Compatible
- Three-State Noninverting Outputs
- Propagation Delay ................. 35ns Max.
- Gated Inputs:
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Low Power Operation ............ ICCSB = 10µA
- Operating Temperature Ranges
  - C82C82 .............. 0°C to +70°C
  - I82C82 ................ -40°C to +85°C
  - M82C82 .............. -55°C to +125°C

Description
The Harris 82C82 is a high performance CMOS Octal Latching Buffer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C82 provides an eight-bit parallel latch/buffer in a 20 pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable (OE) permits simple interface to state-of-the-art microprocessor systems.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP. RANGE</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP82C82</td>
<td>0°C to +70°C</td>
<td>20 Ld PDIP</td>
<td>E20.3</td>
</tr>
<tr>
<td>IS82C82</td>
<td>-40°C to +85°C</td>
<td>20 Ld PLCC</td>
<td>N20.35</td>
</tr>
<tr>
<td>DS82C82</td>
<td>0°C to +70°C</td>
<td>20 Ld PLCC</td>
<td>N20.35</td>
</tr>
<tr>
<td>CS82C82</td>
<td>-40°C to +85°C</td>
<td>20 Ld PLCC</td>
<td>N20.35</td>
</tr>
<tr>
<td>CD82C82</td>
<td>0°C to +70°C</td>
<td>20 Ld CERDIP</td>
<td>F20.3</td>
</tr>
<tr>
<td>MD82C82/B</td>
<td>-40°C to +85°C</td>
<td>20 Pad CLCC</td>
<td>J20.A</td>
</tr>
<tr>
<td>8406701RA</td>
<td>-55°C to +125°C</td>
<td>SMD #</td>
<td></td>
</tr>
<tr>
<td>MR82C82/B</td>
<td>-55°C to +125°C</td>
<td>SMD #</td>
<td></td>
</tr>
<tr>
<td>84067012A</td>
<td>-55°C to +125°C</td>
<td>SMD #</td>
<td></td>
</tr>
</tbody>
</table>

Pinouts

<table>
<thead>
<tr>
<th>PIN NAMES</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DI0-DI7</td>
<td>Data Input Pins</td>
</tr>
<tr>
<td>DO0-DO7</td>
<td>Data Output Pins</td>
</tr>
<tr>
<td>STB</td>
<td>Active High Strobe</td>
</tr>
<tr>
<td>OE</td>
<td>Active Low Output Enable</td>
</tr>
</tbody>
</table>

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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**Functional Diagram**

**Gated Inputs**

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between $V_{CC}$ and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the input and cause a disruption in device operation.

The Harris 82C8X Series of bus drivers eliminates these conditions by turning off data inputs when data is latched ($STB = 0$ for the 82C82/83H) and when the device is disabled ($OE = 1$ for 82C86H/87H). These gated inputs disconnect the input circuitry from the $V_{CC}$ and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figures 1, 2). No new current flow from $V_{CC}$ to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

DC input voltage levels can also cause an increase in $ICC$ if these input levels approach the minimum $V_{IH}$ or maximum $V_{IL}$ conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode ($STB = 1$). $ICC$ remains below the maximum $ICC$ standby specification of 10mA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

**Typical 82C82 System Example**

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 3). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 at 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.
Application Information

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by:

\[ I = C_L \frac{dV}{dt} \]  
\[ \text{(EQ. 1)} \]

Assuming that all outputs change state at the same time and that \( \frac{dV}{dt} \) is constant:

\[ I = C_L \frac{(V_{CC} \times 80\%)}{t_R/t_f} \]  
\[ \text{(EQ. 2)} \]

\[ \text{(EQ. 3)} \]

where \( t_R = 20\text{ns}, V_{CC} = 5.0\text{V}, C_L = 300\text{pF} \) on each of eight outputs.

\[ I = (8 \times 300 \times 10^{-12}) \times (5.0\text{V} \times 0.8)/(20 \times 10^{-9}) = 480\text{mA} \]  
\[ \text{(EQ. 4)} \]

This current spike may cause a large negative voltage spike on \( V_{CC} \), which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1\( \mu \text{F} \) ceramic disc decoupling capacitor be placed between \( V_{CC} \) and GND at each device, with placement being as near to the device as possible.

FIGURE 18. SYSTEM EFFECTS OF GATED INPUTS
Absolute Maximum Ratings

Supply Voltage .............................................. +8.0V
Input, Output or I/O Voltage ............................ GND -0.5V to VCC +0.5V
ESD Classification ....................................... Class 1

Operating Conditions

Operating Voltage Range ................................. +4.5V to +5.5V
Operating Temperature Range
  82C82 ............................................. 0°C to +70°C
  I82C82 ........................................... -40°C to +85°C
  M82C82 .......................................... -55°C to +125°C

Thermal Information

θJA ..................................................... 75°C/W
θJC ..................................................... 18°C/W
CERDIP ................................................ 85°C/W
CLCC ................................................... 22°C/W
PDIP ................................................... 75 N/A
PLCC ................................................... 75 N/A

Storage Temperature Range ................................ -65°C to +150°C

Maximum Junction Temperature
  Ceramic Package ...................................... +175°C
  Plastic Package ..................................... +150°C
  Minimum Lead Temperature (Soldering 10s) ............. +300°C
  (PLCC Lead Tips Only)

Die Characteristics

Gate Count .................................................. 65 Gates

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications  VCC = 5.0V ±10%;

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical One Input Voltage</td>
<td>2.0</td>
<td>-</td>
<td>V</td>
<td>C82C82, I82C82 (Note 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.2</td>
<td>-</td>
<td>V</td>
<td>M82C82 (Note 1)</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical Zero Input Voltage</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical One Output Voltage</td>
<td>2.9</td>
<td>-</td>
<td>V</td>
<td>IOH = -8mA, OE = GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCC -0.4V</td>
<td>-</td>
<td>V</td>
<td>IOH = -100µA, OE = GND</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical Zero Output Voltage</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
<td>IOL = 8mA, OE = GND</td>
</tr>
<tr>
<td>II</td>
<td>Input Leakage Current</td>
<td>-1.0</td>
<td>1.0</td>
<td>µA</td>
<td>VIN = GND or VCC, DIP Pins 1-9, 11</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage Current</td>
<td>-10.0</td>
<td>10.0</td>
<td>µA</td>
<td>VO = GND or VCC, OE ≥ VCC -0.5V DIP Pins 12-19</td>
</tr>
<tr>
<td>ICCSB</td>
<td>Standby Power Supply Current</td>
<td>-</td>
<td>10</td>
<td>µA</td>
<td>VIN = VCC or GND, VCC = 5.5V, Outputs Open</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Power Supply Current</td>
<td>-</td>
<td>1</td>
<td>mA/MHz</td>
<td>TA = +25°C, VCC = 5V, Typical (See Note 2)</td>
</tr>
</tbody>
</table>

NOTES:
1. VIH is measured by applying a pulse of magnitude = VIH min to one data input at a time and checking the corresponding device output for a valid logical “1” during valid input high time. Control pins (STB, OE) are tested separately with all device data input pins at VCC -0.4.
2. Typical ICCOP = 1mA/MHz of STB cycle time. (Example: 5MHz µP, ALE = 1.25MHz, ICCOP = 1.25mA).

Capacitance  TA = +25°C

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TYPICAL</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>13</td>
<td>pF</td>
<td>Freq = 1MHz, all measurements are referenced to device GND</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td>20</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>
**AC Electrical Specifications**  

\[ V_{CC} = 5.0\text{V} \pm 10\%; \quad T_A = 0^\circ\text{C} \text{ to } +70^\circ\text{C} \ (82C82); \]

\[ C_L = 300pF \ (\text{Note 1}), \text{Freq} = 1\text{MHz} \quad T_A = -40^\circ\text{C} \text{ to } +85^\circ\text{C} \ (I82C82); \]

\[ T_A = -55^\circ\text{C} \text{ to } +125^\circ\text{C} \ (M82C82) \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) TIVOV</td>
<td>Propagation Delay Input to Output</td>
<td>-</td>
<td>35</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(2) TSHOV</td>
<td>Propagation Delay STB to Output</td>
<td>-</td>
<td>55</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(3) TEHOZ</td>
<td>Output Disable Time</td>
<td>-</td>
<td>35</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(4) TELOV</td>
<td>Output Enable Time</td>
<td>-</td>
<td>50</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(5) TIVSL</td>
<td>Input to STB Setup Time</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(6) TSLIX</td>
<td>Input to STB Hold Time</td>
<td>25</td>
<td>-</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(7) TSHSL</td>
<td>STB High Time</td>
<td>25</td>
<td>-</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
<tr>
<td>(8) TR, TF</td>
<td>Input Rise/Fall Times</td>
<td>-</td>
<td>20</td>
<td>ns</td>
<td>Notes 2, 3</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Output load capacitance is rated at 300pF for ceramic and plastic packages.
2. All AC parameters tested as per test circuits and definitions below. Input rise and fall times are driven at 1ns/V.
3. Input test signals must switch between \( V_{IL} = -0.4\text{V} \) and \( V_{IH} = +0.4\text{V} \).

**Timing Waveforms**

![Timing Waveforms Diagram]

**Test Load Circuits**

![Test Load Circuits Diagram]

**NOTE:** Includes stray and jig capacitance.
**Burn-In Circuits**

**NOTES:**

1. \( V_{CC} = 5.5 \pm 0.5 \text{V}, \) GND = 0V.
2. \( V_{IH} = 4.5 \text{V} \pm 10\% \).
3. \( V_{IL} = -0.2 \text{V} \) to 0.4V.
4. \( R_1 = 47k \Omega \pm 5\% \).
5. \( R_2 = 2.0k \Omega \pm 5\% \).
6. \( R_3 = 4.2k \Omega \pm 5\% \).
7. \( R_4 = 470k \Omega \pm 5\% \).
8. \( C_1 = 0.01 \mu \text{F} \) minimum.
9. \( F_0 = 100k\text{Hz} \pm 10\% \).
10. \( F_1 = F_0/2, \) \( F_2 = F_1/2 \).
Die Characteristics

DIE DIMENSIONS:
118.1 x 92.1 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±1kÅ

GLASSIVATION:
Type: SiO₂
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.00 x 10⁵ A/cm²

Metallization Mask Layout